AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1. (original)   A programmable logic device comprising
    - a number of logic blocks with configurable characteristics which in each case comprise at least one processing unit with function programs and interfaces to the in each case other logic blocks,
    - at least one input/output unit associated with the logic blocks,

   and
    - means for linking the logic blocks
      a) to one another,
      b) to at least one of the processing units of another logic block and
      c) to the at least one input/output unit, characterized by reconfigurability of the logic blocks (3A to 3D) during the entire operation of the logic device (7), due to the fact that the linking elements additionally exhibit at least one configurable changeover logic block (8) by means of which at least some of the reconfigurable logic blocks (3A to 3D) themselves and/or their connections to one another and/or their connections to the at least one processing unit (4) and/or their connections of the at least one input/output unit (5) are configured.

2. (original)   The device as claimed in claim 1, characterized in that the changeover logic block (8) is

constructed in one plane (E2) which differs from a plane (E1) with the reconfigurable logic blocks (3A to 3D).

3. (original) The device as claimed in claim 2, characterized in that the planes (E1, E2) are constructed at least largely equivalently.

4. (currently amended) The device as claimed in ~~one of the preceding claims~~ claim 1, characterized in that at least some of the reconfigurable logic blocks (3A to 3D) are configured in accordance with a predetermined context (c).

5. (currently amended) The device as claimed in ~~one of the preceding claims~~ claim 1, characterized in that the changeover logic block (8) exhibits at least one state memory which contains information with respect to the functions of the individual reconfigurable logic blocks (3A to 3D), and that the selected reconfigurable logic blocks are configured in accordance with the function information of the selected state.